Features

- Input Voltage Range: 1.1V~5.5V
- Internal MOSFET with high switch current up to 3A
- Shutdown Mode Supply Current: <5μA
- 90% Efficiency
- Up to 450kHz Switching Frequency
- Using Internal Power Switches
- SOT-23-6 Package

Applications

- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instruments
- Wireless Equipments

Description

The AP8362 is a compact, high efficiency, and low voltage step-up DC/DC converter including an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The low start-up input voltage below 1.1V. The high switching rate minimized the size of external components. Besides, the 25μA low quiescent current together with high efficiency maintains long battery lifetime. The output voltage is set with two external resistors.

The AP8362 is available in the industry standard SOT-23-6 power packages.

Typical Application

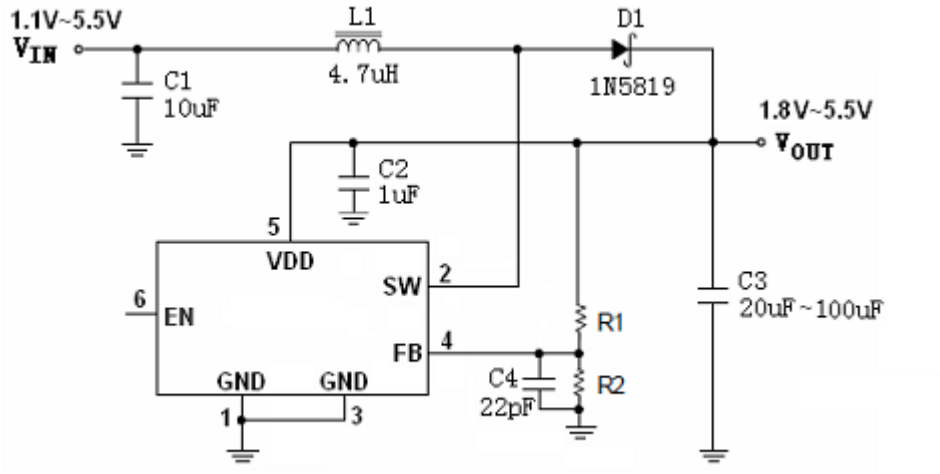


Figure 1: (1.1V Stat-up input Voltage)

Test Circuit

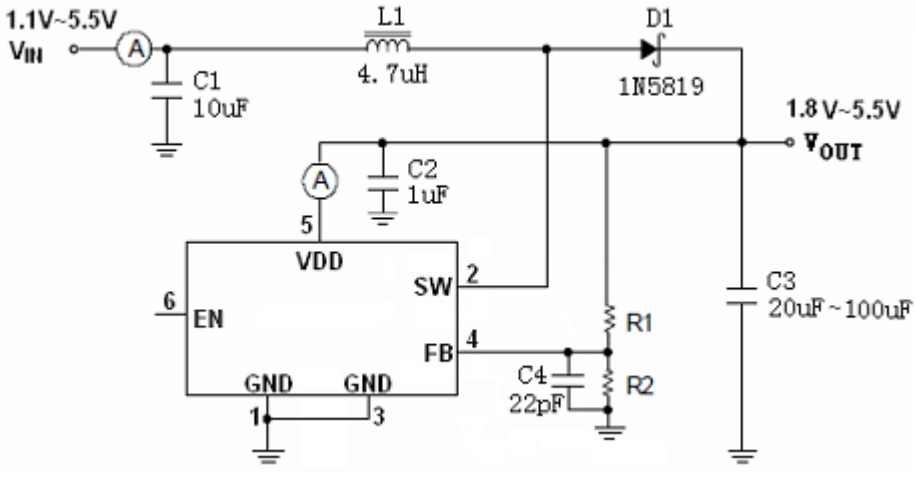


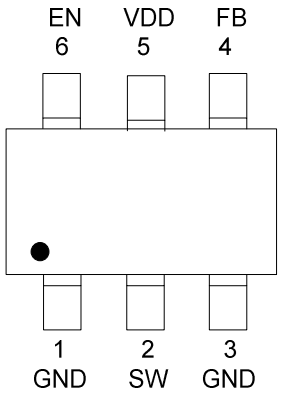
Figure 2: (1.1V Stat-up input Voltage)

Absolute Maximum Ratings (Note 1)

- Supply Voltage……−0.3V to 6V
- SW Pin Switch Voltage……−0.3V to 6V
- Other I/O Pin Voltages……−0.3V to 6V
- SW Pin Switch Current ……..……..4A
- Operating Junction Temperature……..125℃
- Storage Temperature Range ……−65℃ ~ +150℃
- Lead Temperature (Soldering 10 sec.) ……..+ 300℃

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Pin Description



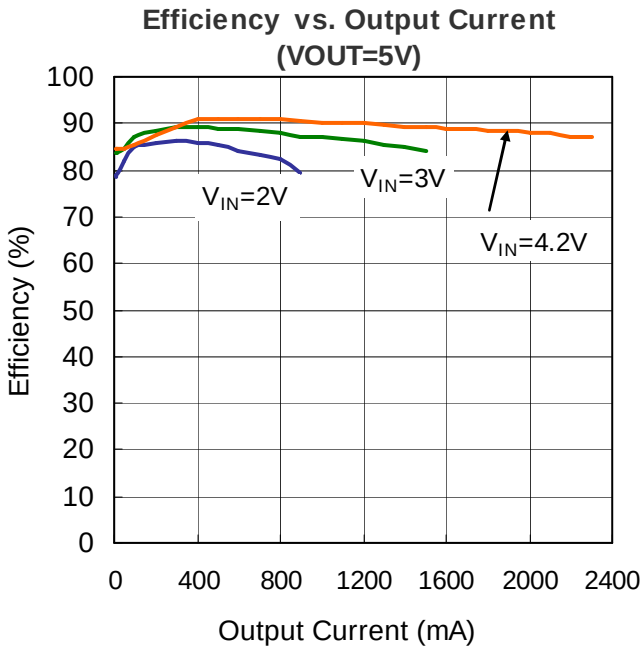
PIN NUMBER SOT23-6	PIN NAME	FUNCTION
1/3	GND	Ground
2	SW	Switch Node for Output
4	FB	Feedback
5	VDD	Output
6	EN	ON/OFF Control(High Enable)

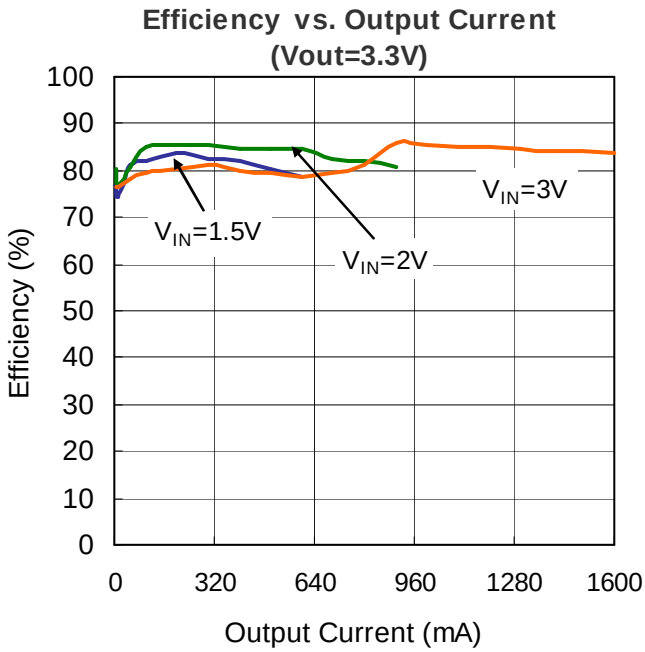
Electrical Characteristics

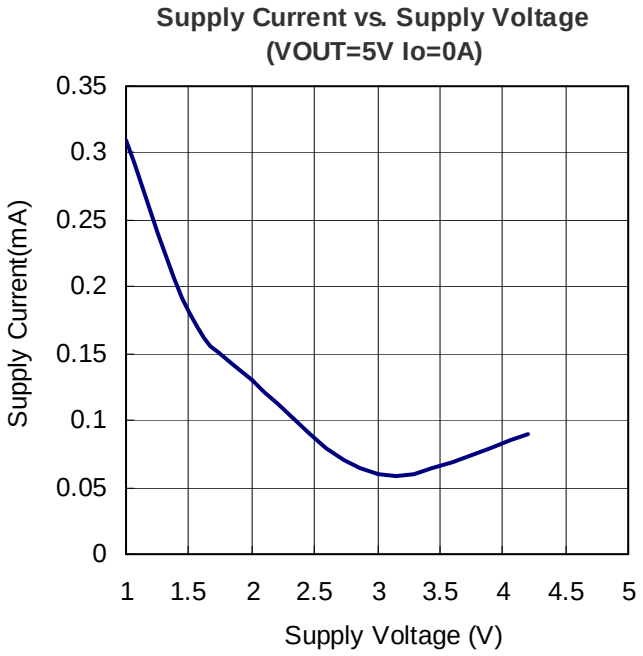
(V_{IN} = 1.5V, VDD set to 3.3V, Load Current = 0A, TA = 25℃, unless otherwise specified)

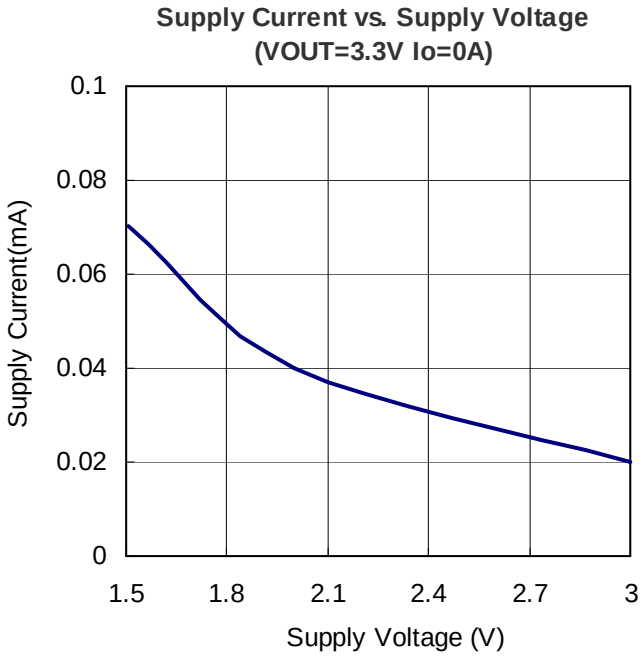
Parameter	Test Conditions	Min	Typ	Max	Units
Start-UP Voltage	IL = 1mA	1.00			V
Operating VDD Range	VDD pin voltage	1.0		5.5	V
No Load Current I (V_{IN})	V_{IN} = 1.5V, V_{OUT} = 3.3V		70		μA
Feedback Reference Voltage	Close Loop, VDD = 3.3V	1.18	1.2	1.22	V
Switching Frequency	VDD = 3.3V		450		KHz
Maximum Duty	VDD = 3.3V		80		%
SW ON Resistance	VDD = 3.3V		0.07		Ω
Current Limit Setting	VDD = 3.3V		3		A
Line Regulation	V_{IN} = 1.5 ~ 2.5V, IL = 100mA		25		mV/V
Load Regulation	V_{IN} = 2.5V, IL = 1 ~ 300mA		0.05		mV/mA
En Input High		1			V
En Input Low				0.6	V
Temperature Stability for V_{OUT}			50		ppm/℃
Thermal Shutdown			165		℃
Maximum V_{RM}			145		mV

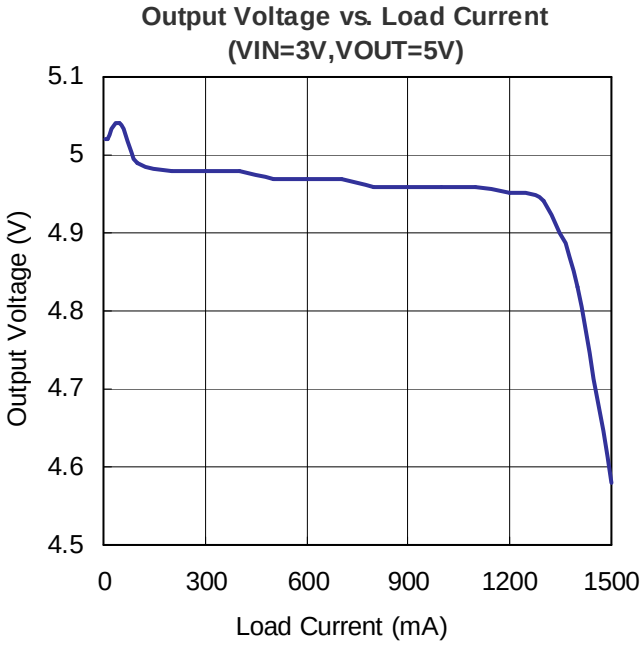
Typical Performance Characteristics

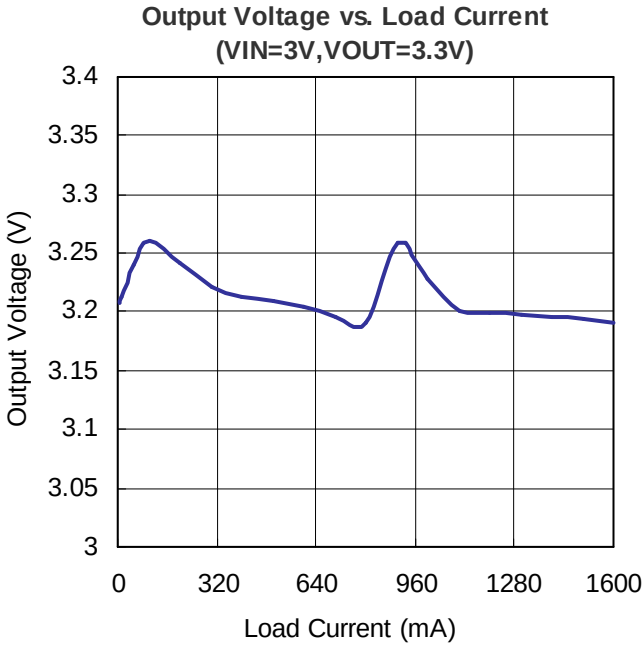












Pin Information

GND (Pin 1/3): Signal and Power Ground. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s).

SW (Pin 2): Switch Pin. Connect inductor between SW and V_{IN}. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

FB (Pin 4): Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.8V to 5.5V by: $V_{OUT} = 1.2V \bullet [1 + (R1/R2)]$

VDD (Pin 5): Input positive power pin.

EN (Pin 6): En Control Input. Forcing this pin above 1V enables the part. Forcing this pin below 0.6V shuts down the device. In shutdown, all functions are disabled, drawing <1μA supply current. Do not leave EN floating.

Operation

The AP8362 are 450kHz, High Efficiency, Step-up DC/DC Converter housed in a 6-lead ThinSOT package. Able to operate from an input voltage below 1V, the devices feature fixed frequency, current mode PWM control for exceptional line and load regulation. With its low RDS(ON) and gate charge internal MOSFET switches, the devices maintain high efficiency over a wide range of load current. Detailed descriptions of the three distinct operating modes follow. Operation can be best understood by referring to the Block Diagram.

Low Voltage Start-Up

The AP8362 will start up at a typical VIN voltage of 0.9V or higher. The low voltage start-up circuitry controls the internal NMOS switch up to a maximum peak inductor current of 850mA (typ), with an approximate 1.5ms off-time during start-up, allowing the devices to start up into an output load. Once VOUT exceeds 2.3V, the start-up circuitry is disabled and normal fixed frequency PWM operation is initiated. In this mode, the AP8362 operate independent of VIN, allowing extended operating time as the battery can droop to several tenths of a volt without affecting output voltage regulation. The limiting factor for the application becomes the ability of the battery to supply sufficient energy to the output.

Low Noise Fixed Frequency Operation

Oscillator: The frequency of operation is internally set to 0.45kHz. Error Amp: The error amplifier is an internally compensated transconductance type (current output) with a transconductance (gm) = 33 microsiemens. The internal 1.212V reference voltage is compared to the voltage at the FB pin to generate an error signal at the output of the error amplifier. A voltage divider from VOUT to ground programs the output voltage via FB from 2.5V to 5V using the equation: VOUT = 1.212V • [1 + (R1/R2)] Current Sensing: A signal representing NMOS switch current is summed with the slope compensator. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM.

Peak switch current is limited to approximately 3A independent of input or output voltage. The current signal is blanked for 40ns to enhance noise rejection. Antiringing Control: The antiringing control circuitry prevents high frequency ringing of the SW pin as the inductor current goes to zero by damping the resonant circuit formed by L and C_{SW} (capacitance on SW pin).

Burst Mode Operation

Portable devices frequently spend extended time in low power or standby mode, only switching to high power drain when specific functions are enabled. In order to improve battery life in these types of products, high power converter efficiency needs to be maintained over a wide output power range. In addition to its high efficiency at moderate and heavy loads, the AP8362 includes automatic Burst Mode operation that improves efficiency of the power converter at light loads. Burst mode operation is initiated if the output load current falls below an internally programmed threshold. Once initiated, the Burst Mode operation circuitry shuts down most of the device, only keeping alive the circuitry required to monitor the output voltage. This is referred to as the sleep state. In sleep, the AP8362 draws only 19uA from the output capacitor, greatly enhancing efficiency.

When the output voltage has drooped approximately 1% from nominal, the AP8362 wakes up and

commences normal PWM operation. The output capacitor recharges and causes the AP8362 to reenter sleep if the output load remains less than the sleep threshold. The frequency of this intermittent PWM or burst operation is proportional to load current; that is, as the load current drops further below the burst threshold, the AP8362 turns on less frequently. When the load current increases above the burst threshold, the AP8362 will resume continuous PWM operation seamlessly. Referring to the Block Diagram, an optional capacitor (C_{FF}) between VOUT and FB in some circumstances can reduce the peak-to-peak VOUT ripple and input quiescent current during Burst Mode operation. Typical values for C_{FF} range from 15pF to 220pF. The AP8362 does not use Burst Mode operation and features continuous operation at light loads, eliminating low frequency output voltage ripple at the expense of light load efficiency.

Application Information

Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7µH to 10µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation 1. A reasonable starting point for setting ripple current is $\triangle I_L$ = 0.92A (40% of 2.3A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 3A rated inductor should be enough for most applications (2.3A + 0.46A). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the AP8362 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the

capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. The Table 1 shows the suggested C_{IN} and C_{OUT}.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge △Q moves from VIN to ground. The resulting △Q/△t is the current out of VIN that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the

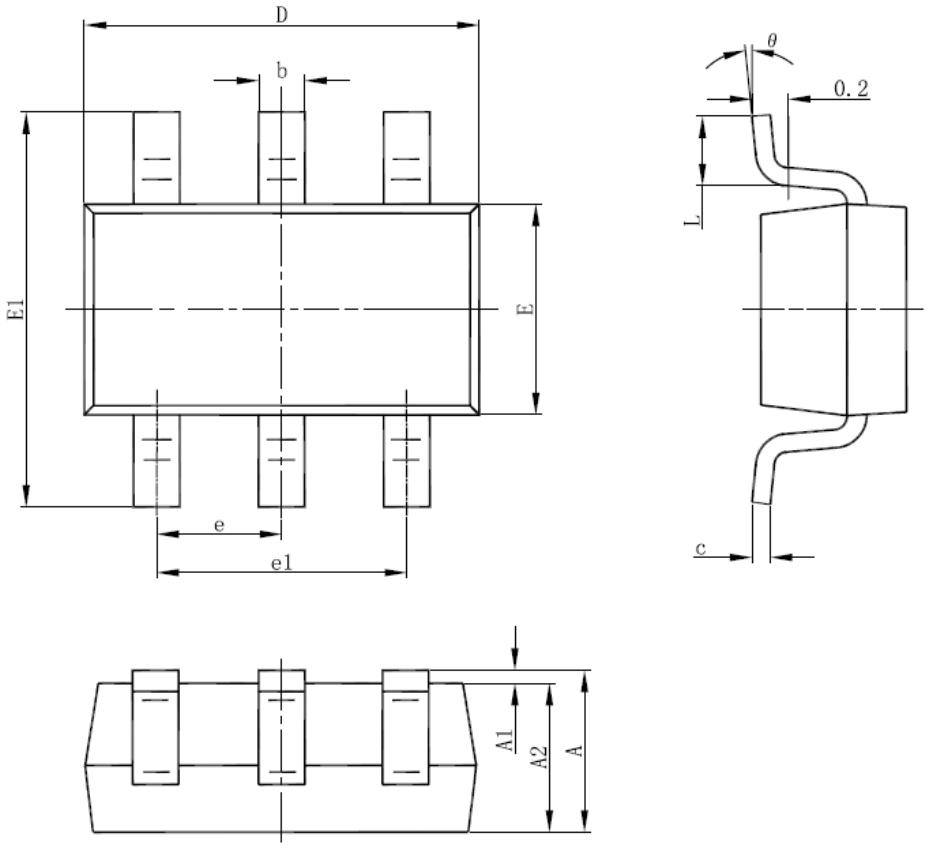
main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Table 1: Suggested Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (uF)	Case Size
TDK	C1608JB0J475M	4.7	0603
TDK	C2012JB0J106M	10	0805
MURATA	GRM188R60J475KE19	4.7	0603
MURATA	GRM219R60J106ME19	10	0805
MURATA	GRM219R60J106KE19	10	0805
TAIYO YUDEN	JMK107BJ475RA	4.7	0603
TAIYO YUDEN	JMK107BJ106MA	10	0603
TAIYO YUDEN	JMK212BJ106RD	10	0805

Packaging Information

SOT-23-6 Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°